# ECED 4260 IC design and Fabrication

## Assignment #1 Reference Solution
## http://myweb.dal.ca/~jgu/4260/assignments.html

Assignment #1 contains the following problems:

1) Prove the following simplification theorems using the first eight laws of Boolean algebra. Explain each step

   (X+Y)(X+Y')=X

   (X+Y)(X+Y')
   =XX+XY'+YX+YY'
   =X+X(Y'+Y)+0
   =X+X(1)
   =X

   X(X+Y)=X

   X(X+Y)
   =XX+XY
   =X+XY
   =X(1+Y)
   =X(1)
   =X

   (X+Y')Y=XY

   (X+Y')Y
   =XY+Y'Y
   =XY+0
   =XY

   (X+Y)(X'+Z)=XZ+X'Y

   (X+Y)(X'+Z)
   =XX'+XZ+YX'+YZ
   =0+XZ+YX'+YZ
   =XZ+YX'+(X+X')YZ
   =XZ+XYZ+YX'+YX'Z
   =XZ+X'Y

2) Simplify the following functions using the theorems of Boolean algebra.

   a. f(X,Y)=XY+XY'
   =X(Y+Y')
   =X(1)
   =X

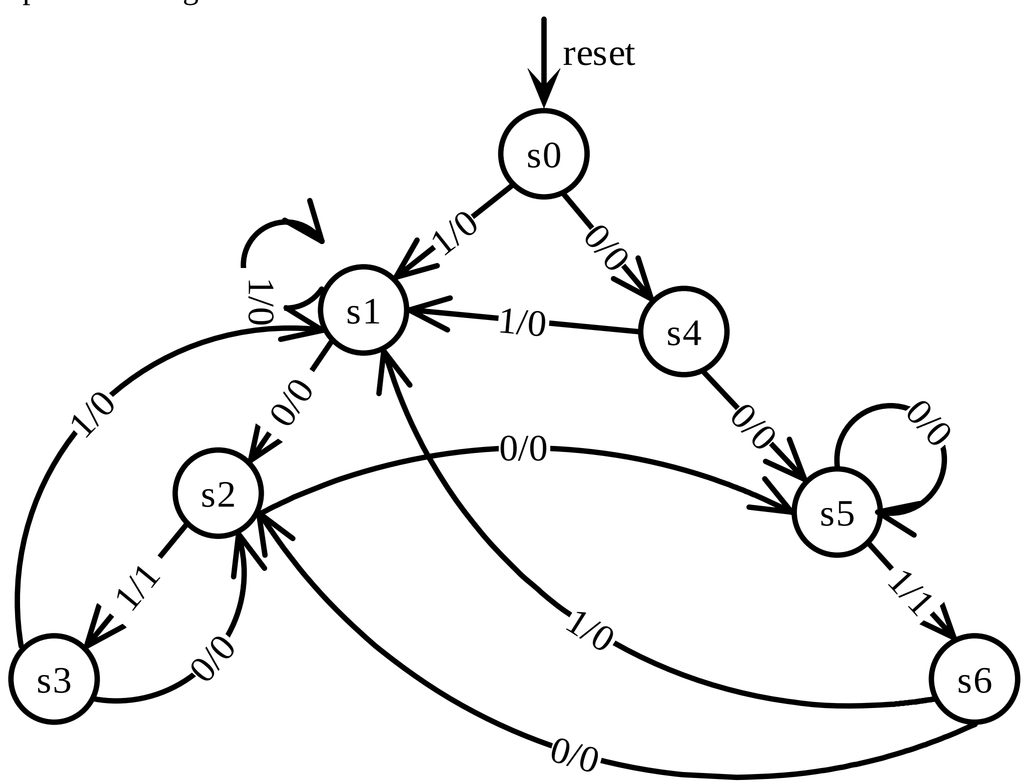
b. f(X,Y)=(X+Y)(X+Y’)
=XX+XY’+YX+YY’
=X+X(Y+Y’)+0
=X+X
=X

c. f(X,Y,Z)=YZ’+X’YZ+XYZ
=YZ’+(X’+X)YZ
=YZ’+YZ
=Y(Z+Z’)
=Y(1)
=Y

d. f(X,Y,Z)=(X+Y)(X’+Y+Z)(X’+Y+Z’)
=(X+Y)(X’+Y) from b
=Y

e. f(W,X,Y,Z)=X+XYZ+X’YZ+X’Y+WX+W’X
=X+X’Y+(W+W’)X
=X+X’Y+X
=X+X’Y

3) Design a mealy sequential circuit with one input and one output which detects instances of the patterns “101” and “001”, including overlapping patterns.
Step1: State diagram:



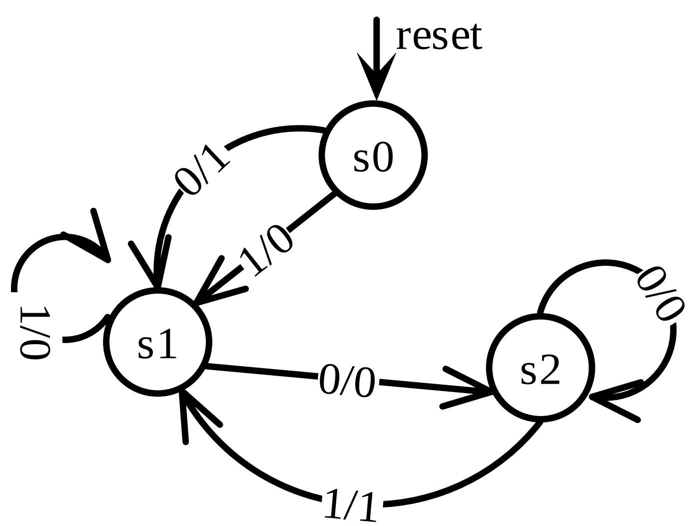
Derive the symbolic table:

| Present | Next state | | Output | |
|---|---|---|---|---|
| State | X=0 | X=1 | X=0 | X=1 |
| S0 | S4 | S1 | 0 | 0 |
| S1 | S2 | S1 | 0 | 0 |
| S2 | S5 | S3 | 0 | 1 |
| S3 | S2 | S1 | 0 | 0 |
| S4 | S5 | S1 | 0 | 0 |
| S5 | S5 | S6 | 0 | 1 |
| S6 | S2 | S1 | 0 | 0 |

Step 2: Reduced table:

| | | | | | | |
|---|---|---|---|---|---|---|
| S1 | 2-4 | | | | | |
| S2 | X | X | | | | |
| S3s | 2-4 | Ok | X | | | |
| S4 | 5-4 | 2-5 | X | 2-5 | | |
| S5 | X | X | 6-3 | X | X | |
| S6 | 2-4 | Ok | X | ok | 2-5 | X |
| | S0 | S1 | S2 | S3 | S4 | S5 |

| Present | Next state | | Output | |
|---|---|---|---|---|
| State | X=0 | X=1 | X=0 | X=1 |
| S0 | S1 | S1 | 0 | 0 |
| S1 | S2 | S1 | 0 | 0 |
| S2 | S2 | S1 | 0 | 1 |



step3: state assignment:

1) States that have the same next state for a given input

   {S0 S1}
2) States that are the next states of the same state
   {S1, S2}
3) States that have the same output for the same input.
   {S1,S2}

State assignment: S0: 00 , S1:01, s2:11

Step 4: construct the binary state table:

| Present | Next state | | Output | |
|---|---|---|---|---|
| State | X=0 | X=1 | X=0 | X=1 |
| 00 | 01 | 01 | 0 | 0 |
| 01 | 11 | 01 | 0 | 0 |
| 11 | 11 | 01 | 0 | 1 |

Step 5,6: find minimum flip-flop input & output functions

| B \ XA | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | Φ | Φ | 0 |
| 1 | 1 | 1 | 0 | 0 |

A+

| B \ XA | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | Φ | Φ | 1 |
| 1 | 1 | 1 | 1 | 1 |

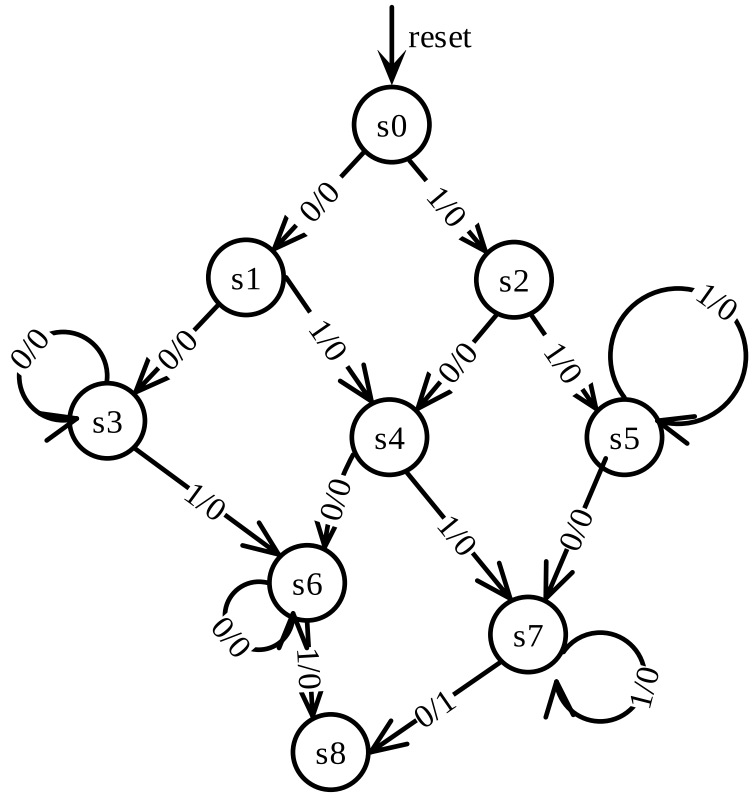
B+

| B \ XA | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | Φ | Φ | 0 |
| 1 | 0 | 0 | 1 | 0 |

output

$\overline{A^{+}}=\overline{B}+X$ $B^{+}=1$ output=AX

4) A finite state machine has one input and one output. The output becomes 1 and remains 1 thereafter when at least two 0's and at least two 1's have occurred as inputs, regardless of the order of occurrence. Assuming this is to be implemented as a moore machine, draw a state diagram. (8.13)




5) Reduce the number of states in the following state table to the minimum number required.

| Present | Next state | | Output |
|---|---|---|---|
| State | X=0 | X=1 | |
| S0 | S5 | S2 | 0 |
| S1 | S3 | S5 | 0 |
| S2 | S7 | S0 | 0 |
| S3 | S1 | S6 | 0 |
| S4 | S6 | S5 | 1 |
| S5 | S0 | S6 | 0 |
| S6 | S4 | S7 | 1 |
| S7 | S2 | S4 | 0 |

Reduced table:

| Present | Next state | | Output |
|---|---|---|---|
| | X=0 | X=1 | |
| S0 | S5 | S0 | 0 |
| S1 | S3 | S5 | 0 |
| S3 | S1 | S4 | 0 |
| S4 | S4 | S5 | 1 |
| S5 | S0 | S4 | 0 |