

ECED 4260 IC Design and Fabrication

Assignment #2

<http://myweb.dal.ca/~jgu/4260/assignments.html>

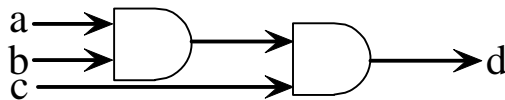
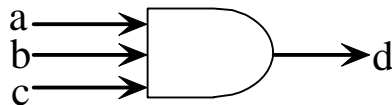
Due date: Oct. 20 2011. Late submission will not be accepted.

Assignment #2 contains the following problems:

- 1) Which of the following are valid VHDL basic identifiers? Which are reserved words?

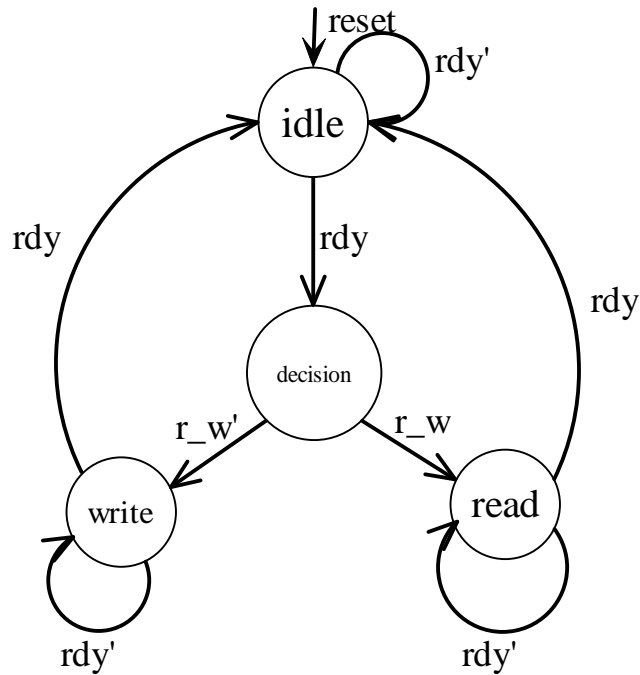
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This_is_one #5_isnot How_about_this_one Last_one

- 2) Write a while loop that sums the positive integers from 1 to 1000.
- 3) Write an array type declaration for an array of 10 integers, and a variable declaration for a variable of the type. Write a for loop to calculate the product of the array elements.
- 4) Write entities and architectures, which describe the circuits shown below. For the first one, just use Boolean algebra. For the second one, you are required to construct a two input and gate and use component instantiation to build the three input and gate.



- 5) A finite state machine is shown below, and the output table is provided. Write architecture of this state machine.

State	Outputs	
	Oe	We
Idle	0	0
Decision	0	0
Write	0	1
Read	1	0



- 6) Write two functions, one to find the maximum value in an array of integers and the other to find the minimum value
- 7) Draw a timing diagram which illustrate the difference between the following VHDL statements

Signal a, b, c, d: bit;
 B <= a after 5 ns;
 C <= transport a after 5 ns;
 D <= reject 3ns inertial a after 5 ns;

