

# ECED 4260 IC Design and Fabrication

## Assignment #3

<http://myweb.dal.ca/~jgu/4260/assignments.html>

Due date: Nov. 17 2011. Late submission will not be accepted.

Plot F1 & F2 into the map and read them out

A	B	C	D	F1	F2
0	0	0	0	Φ	0
0	0	0	1	Φ	0
0	0	1	0	1	Φ
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	1
0	1	1	0	Φ	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	Φ	Φ
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	1	Φ
1	1	1	0	0	1
1	1	1	1	Φ	0

C \ AB	00	01	11	10
0				
1				

C \ AB	00	01	11	10
0				
1				

C \ AB	00	01	11	10
0				
1				

C \ AB	00	01	11	10
0				
1				