

# ECED 4260 IC Design and Fabrication

## Assignment #4

<http://myweb.dal.ca/~jgu/4260/assignments.html>

**Due date: Dec. 1 2011. Late submission will not be accepted.**

Assignment #4 contains the following problems:

- 1) Convert the following binary numbers to decimal numbers; using each of unsigned, sign and magnitude, one's complement, and two's complement representation.

011011, 1010101, 10100011110000

- 2) Convert the following decimal numbers into two's complement representation binary numbers -1023, 1998, 88888, -9999
- 3) Calculate the worst-case delay of a 6-bit adder built with a two 3-bit carry look-ahead adders and a carry look-ahead generator.
- 4) Multiply the following numbers using Booth multiplication and fast (modified booth) multiplication. Show all partial products:

10100101110, 11000101110

- 5) For each pair of IEEE 754 single precision floating point numbers, find their sum and product expressed in IEEE 754 using the algorithms shown in class. Express the given numbers in decimal as well:

A)

1	10000000	100000000000000000000000
0	10000001	110000000000000000000000

B)

0	01100000	010100000000000000000000
0	01100000	010110000000000000000000